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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,677	10/11/2001	Mark Boike	01-373/4028-00800	9455

7590 06/28/2004

Intellectual Property Law Department
LSI Logic Corporation
Mail Stop D-106
1551 McCarthy Boulevard
Milpitas, CA 95035

EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,677	BOIKE ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-10,13,14,18 and 20* is/are rejected.

7)☒ Claim(s) *4-6,11,12,15-17,19,21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 18 recites the limitation "each direct memory access device" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3,8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Skapura (patent No. 5,204,938) in view of Morton (patent No. 5,822,606).

5. Skapura taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Plurality of digital signal processors (10a,10b,10c,10d) (e.g., see fig.3);

b) Host interface (26,27) coupled to a host processor (40) and the plurality of digital processors (e.g., see fig. 3).

6. Skapura did not expressly detail (claim 1) that the system elements were on an integrated circuit. Morton however taught (e.g., see fig.1 and col. 6, lines 9-60) a parallel DSP chip. It would have been obvious to one of ordinary skill to combine the

teachings of Skapura and Morton. One of ordinary skill would have been motivated to incorporate the teaching of Morton of implementing the parallel DSP system as integrated circuit at least for the reasons taught by Morton (e.g., see col. 1, lines 64-col. 2, line16) such as the advantage of the parallel semiconductor chip was to improve the rate at which data was processed at low cost, consuming minimum power and occupying minimum space.

7. As per claim 2, Skapura taught a plurality of memory devices (17a, 17b, 17c, 17d) each associated with and coupled to one of the plurality of digital signal processors and each coupled to the host processor interface (e.g., see fig. 3).

8. As per claim 3, Skapura taught a memory bus (23) coupling each of the memory devices with the host processor interface (e.g., see fig. 3). As to the limitation of claim 8, one ordinary skill would have been required to utilize DSPs to implement the system Skapura and Morton.

9. As to the limitations of claims 8, one of ordinary skill would have been motivated to utilize a particular model DSP such as the ZSP400 depending on the cost and performance of the standard DSP versus other standard processors.

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Skapura and Morton as applied to claims 1-3 above, and further in view of Swoboda (patent No. 6,643,803).

11. Morton taught a debug port (e.g., see col. 6, lines 40-43). But did not particularize the type of debug system coupled to the system. Swoboda taught a test system (870)

for emulating the DSP the used the IEEE 1149.1 standard test access port and boundary scan architecture (e.g., see col. 4, lines 23-51).

12. It would have been obvious to one of ordinary skill to combine the teachings of Skapura and Swoboda. One of ordinary skill would have been motivated to incorporate the teachings of Swoboda at least to enable debug of the system to ensure proper operation.

13. Claim 9,10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morton (patent No. 5,822,606).

14. Morton taught the invention substantially as claimed including a data processing ("DP") system comprising: and integrated circuit comprising a plurality of digital signal processors (e.g., see fig.1 and col. 6, lines 9-65). Morton did not expressly detail that the DSPs comprised model ZSP400. One of ordinary skill would have been motivated to utilize a particular model DSP such as the ZSP400 depending on the cost and performance of the standard DSP versus other standard processors. As per claim 10, Morton taught a host processor interface (109) coupled to the plurality of signal processors (e.g., see fig. 1).

15. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morton as applied to claims 9,10 above, and further in view of Swoboda (patent No. 6,643,803).

16. Morton taught a debug port (e.g., see col. 6, lines 40-43). But did not particularize the type of debug system coupled to the system. Swoboda taught a test system (870) for emulating the DSP the used the IEEE 1149.1 standard test access port and boundary scan architecture (e.g., see col. 4, lines 23-51).

17. It would have been obvious to one of ordinary skill to combine the teachings of Morton and Swoboda. One of ordinary skill would have been motivated to incorporate the teachings of Swoboda at least to enable debug of the system to ensure proper operation.

18. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morton (patent No. 5,822,606).

19. Morton taught the invention as claimed including a data processing ("DP") system comprising: Means and method of operating at least two digital signal processors (110-113) on a single integrated circuit comprising: coupling the at least two digital signal processors to a host processor using a single host interface (109) (e.g., see fig. 1 and col. 6, lines 9-col. 8, line 34). Morton did not expressly detail the ZSP400 model DSP. As to the limitations of claim 20, one of ordinary skill would have been motivated to utilize a particular model DSP such as the ZSP400 depending on the cost and performance of the standard DSP versus other standard processors.

Claim Rejections - 35 USC § 102

20. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

21. Claim 14 is rejected under 35 U.S.C. 102(b) as being anticipated by Morton (patent No. 5,822,606).

22. Morton taught the invention as claimed including a data processing ("DP") system comprising: Means and method of operating at least two digital signal processors (110-113) on a single integrated circuit comprising: coupling the at least two digital signal processors to a host processor using a single host interface (109) (e.g., see fig. 1 and col. 6, lines 9-col. 8, line 34).

Allowable Subject Matter

23. Claims 4-6,11,12,15-17,19,21,22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Andrews disclosed including a host processor and communications adapter interconnected with a bus (e.g., see abstract).

Hulen disclosed multi-media interface (e.g., see abstract).

Shepard disclosed a serial to parallel and parallel to serial converter for a digital audio workstation (e.g., see abstract).

Yamazaki disclosed a system comprising a DSP on an integrated circuit (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER

June 23, 2004